Zhuolun (Leon) He

Assistant Professor, Department of Computer Science and Technology
Tsinghua University

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Research Interests

Artificial intelligence for electronic design automation: agentic EDA, knowledge representation and formal modeling, large-scale automated reasoning and theorem proving, netlist representation learning, and efficient physical verification.

Academic Appointments

Tsinghua University — Beijing, China
Assistant Professor — *Oct. 2026 – Present*

The Chinese University of Hong Kong — Hong Kong
Postdoctoral Fellow — *Nov. 2023 – Oct. 2026*

Education

The Chinese University of Hong Kong — Hong Kong
Ph.D. in Computer Science and Engineering — *Aug. 2019 – Aug. 2023*

Supervisor: Prof. Bei Yu
Thesis: The Trio of Learning, Optimization, and Acceleration for Efficient Electronic Design Automation

Peking University — Beijing, China
Doctoral studies in Computer Architecture — *Sept. 2017 – Sept. 2018*

Supervisor: Prof. Guojie Luo

Peking University — Beijing, China
B.S. in Computer Science and Technology — *Sept. 2013 – Jul. 2017*

Thesis: Architecture Support for Monadic Serial Dynamic Programming Algorithm

Honors and Awards

- Best Paper Award Nomination, ISPD — 2025
- Best Paper Award Nomination, ICCAD — 2024
- Best Paper Award Nomination, ISPD — 2024
- Third Place, ISPD Contest — 2020
- Champion, EDAthon — 2018
- 2nd Prize (Enterprise Track) — 2025
  8th China Graduate IC Innovation Contest
- 3rd Prize (Team Competition) — 2025
  8th China Graduate IC Innovation Contest
- Outstanding Dissertation Award, School of EECS, Peking University — 2017

Publications

Journal Articles

[J13] Yuqi Jiang, Qian Jin, Xudong Lu, Xiangyue Lyu, **Zhuolun He**, Xunzhao Yin, Yali Fu, Dawei Gao, Bei Yu, Qi Sun, Hanming Wu, and Cheng Zhuo. FabGPT: An Efficient Large Multimodal Model for Complex Wafer Defect Knowledge Queries. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), 2026.

[J12] Fangzhou Liu, Wuqian Tang, Zehua Pei, Ziyang Yu, Haisheng Zheng, **Zhuolun He**, Mengjia Dai, Tinghuan Chen, and Bei Yu. CB-EVO: Contextual Bandit Tuning with Evolutionary Search for Logic Synthesis. *ACM Transactions on Design Automation of Electronic Systems* (*TODAES*), 2026.

[J11] Siting Liu, Jieya Zhou, Jiaxi Jiang, **Zhuolun He**, Ziyi Wang, Yibo Lin, Bei Yu, and Martin Wong. Routing-aware Legal Hybrid Bonding Terminal Assignment for 3D Face-to-Face Stacked ICs. *ACM Transactions on Design Automation of Electronic Systems* (*TODAES*), 2026.

[J10] Yuan Pu, **Zhuolun He**, Yuqi Jiang, Tairu Qiu, Haoyuan Wu, Qi Sun, Cheng Zhuo, and Bei Yu. Customized Retrieval Augmented Generation and Benchmarking for EDA Tool Documentation QA. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), 2025.

[J9] **Zhuolun He**, Yuan Pu, Haoyuan Wu, Tairu Qiu, and Bei Yu. Large Language Models for EDA: Future or Mirage? *ACM Transactions on Design Automation of Electronic Systems* (*TODAES*), 2025. *Editor's Pick*.

[J8] Jiahao Xu, **Zhuolun He**, Shuo Yin, Yuan Pu, Wenjian Yu, and Bei Yu. EasyMRC: Efficient Mask Rule Checking via Representative Edge Sampling. *ACM Transactions on Design Automation of Electronic Systems* (*TODAES*), 2025.

[J7] Yuan Pu, Tinghuan Chen, **Zhuolun He**, Jiajun Qin, Chen Bai, Haisheng Zheng, Yibo Lin, and Bei Yu. IncreMacro: Incremental Macro Placement Refinement. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), 2025.

[J6] **Zhuolun He**, Yuan Pu, Haoyuan Wu, Yuhan Qin, Tairu Qiu, and Bei Yu. Large Language Models for EDA: From Assistants to Agents. *Foundations and Trends in Electronic Design Automation*, 2025.

[J5] Ziyi Wang, Chen Bai, **Zhuolun He**, Guangliang Zhang, Qiang Xu, Tsung-Yi Ho, Yu Huang, and Bei Yu. FGNN2: A Powerful Pre-training Framework for Learning the Logic Functionality of Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), 2025.

[J4] Haoyuan Wu, **Zhuolun He**, Xinyun Zhang, Xufeng Yao, Su Zheng, Haisheng Zheng, and Bei Yu. ChatEDA: A Large Language Model Powered Autonomous Agent for EDA. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), 2024.

[J3] Bizhao Shi, Jiaxi Zhang, **Zhuolun He**, Xuechao Wei, Sicheng Li, Guojie Luo, Hongzhong Zheng, and Yuan Xie. Efficient Super-Resolution System with Block-wise Hybridization and Quantized Winograd on FPGA. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), 2023.

[J2] Ziyi Wang, **Zhuolun He**, Chen Bai, Haoyu Yang, and Bei Yu. Efficient Arithmetic Block Identification with Graph Learning and Network-flow. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), 2023.

[J1] Ching-Yun Ko, Cong Chen, **Zhuolun He**, Yuke Zhang, Kim Batselier, and Ngai Wong. Deep Model Compression and Inference Speedup of Sum-Product Networks on Tensor Trains. *IEEE Transactions on Neural Networks and Learning Systems* (*TNNLS*), 2019.

Conference Papers

[C44] Yuhan Qin, Yuan Pu, **Zhuolun He**, and Bei Yu. FormalPCell: Formal DRC Verification of Parameterized Layout Cells via Symbolic Interpretation and SMT Solving. *IEEE/ACM Asian and South Pacific Design Automation Conference* (*ASPDAC*), Tokyo, Japan, Jan. 25–28, 2027. *To appear*.

[C43] Yuan Pu, Yudong He, Zhenghao Chen, Mingjun Wang, Bingkun Yao, Zhaotan Lin, Qin Chen, Bing Li, Song Chen, **Zhuolun He**, Wenjian Yu, Yanfeng Li, and Bei Yu. ChatFCM: Comprehension-Synthesis Decoupling for LLM-Based Functional Coverage Model Generation. *IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD*), San Jose, CA, USA, Nov. 8–12, 2026.

[C42] Yuheng Huang, Yuhan Qin, Yuan Pu, Zhaotan Lin, Yuntao Nie, **Zhuolun He**, Jianwang Zhai, Kang Zhao, and Bei Yu. A Multi-Granularity Retrieval Augmented Generation Framework for EDA Tasks Leveraging Knowledge Graph. *IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD*), San Jose, CA, USA, Nov. 8–12, 2026.

[C41] Siyang Chen, Yuan Pu, Yuhan Qin, Zhaotan Lin, Siyuan Liang, **Zhuolun He**, Lining Zhang, and Bei Yu. SGLayout: Schema-Guided Closed-Loop Refinement for LLM-Driven Parameterized Layout Generation. *IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD*), San Jose, CA, USA, Nov. 8–12, 2026.

[C40] Rui Ming, Haoyuan Wu, Shoubo Hu, **Zhuolun He**, and Bei Yu. One-Token Rollout: Guiding Supervised Fine-Tuning of LLMs with Policy Gradient. *Empirical Methods in Natural Language Processing* (*EMNLP*), Budapest, Hungary, Oct. 24–29, 2026.

[C39] Mingzi Wang, Lancheng Zou, Shuo Yin, **Zhuolun He**, and Bei Yu. S-Quant: Rethinking Weight Quantization with Seed-Based Generation. *International Conference on Machine Learning* (*ICML*), Seoul, South Korea, July 6–11, 2026.

[C38] Zhenghao Chen, Yuan Pu, Hairuo Han, Yuntao Nie, Jiajun Qin, Yuhan Qin, Tairu Qiu, **Zhuolun He**, Jianwang Zhai, Bei Yu, and Kang Zhao. MAEDA: An LLM-Powered Multi-Agent Evaluation Framework for EDA Tool Documentation QA. *IEEE/ACM Proceedings Design, Automation and Test in Europe* (*DATE*), Verona, Italy, Apr. 20–22, 2026.

[C37] Yuhan Qin, Yuan Pu, Tairu Qiu, **Zhuolun He**, and Bei Yu. Infusing EDA Knowledge into LLM Systems: An Information-Source Perspective. *ACM International Symposium on Physical Design* (*ISPD*), Bonn, Germany, Mar. 15–18, 2026. *Invited Paper*.

[C36] Haisheng Zheng, **Zhuolun He**, Shuo Yin, Yuzhe Ma, and Bei Yu. CombRewriter: Enabling Combinational Logic Simplification in MLIR-Based Hardware Compiler. *IEEE/ACM Asian and South Pacific Design Automation Conference* (*ASPDAC*), Hong Kong, Jan. 19–22, 2026.

[C35] Haoyuan Wu, Rui Ming, Jilong Gao, Hangyu Zhao, Xueyi Chen, Yikai Yang, Haisheng Zheng, **Zhuolun He**, and Bei Yu. On-Policy Optimization with Group Equivalent Preference for Multi-Programming Language Understanding. *Neural Information Processing Systems* (*NeurIPS*), San Diego, CA, USA, Dec. 2–7, 2025.

[C34] Yuan Pu, Yuhao Ji, Siying Yu, Zuodong Zhang, Zizheng Guo, **Zhuolun He**, Yibo Lin, David Z. Pan, and Bei Yu. GPU Acceleration for Versatile Buffer Insertion. *IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD*), Munich, Germany, Oct. 26–30, 2025.

[C33] Yuan Pu, **Zhuolun He**, Shutong Lin, Jiajun Qin, Xinyun Zhang, Hairuo Han, Haisheng Zheng, Yuqi Jiang, Cheng Zhuo, Qi Sun, David Z. Pan, and Bei Yu. MM-GRADE: A Multi-Modal EDA Tool Documentation QA Framework Leveraging Retrieval Augmented Generation. *IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD*), Munich, Germany, Oct. 26–30, 2025.

[C32] Haoyuan Wu, Rui Ming, Haisheng Zheng, **Zhuolun He**, and Bei Yu. Efficient OpAmp Adaptation for Zoom Attention to Golden Contexts. *Association for Computational Linguistics* (*ACL*), Vienna, Austria, July 27–Aug. 1, 2025.

[C31] Haisheng Zheng, Haoyuan Wu, and **Zhuolun He**. ChatLS: Multimodal Retrieval-Augmented Generation and Chain-of-Thought for Logic Synthesis Script Customization. *ACM/IEEE Design Automation Conference* (*DAC*), San Francisco, CA, USA, June 22–25, 2025.

[C30] Hang Liu, Hao Geng, **Zhuolun He**, Qi Sun, and Cheng Zhuo. Swift or Exact? Boosting Efficient Microarchitecture DSE via Multi-fidelity Partial Order Prediction. *ACM/IEEE Design Automation Conference* (*DAC*), San Francisco, CA, USA, June 22–25, 2025.

[C29] Haoyuan Wu, Haisheng Zheng, **Zhuolun He**, and Bei Yu. Divergent Thoughts toward One Goal: LLM-based Multi-Agent Collaboration System for Electronic Design Automation. *Nations of the Americas Chapter of the Association for Computational Linguistics* (*NAACL*), Albuquerque, NM, USA, Apr. 29–May 2, 2025.

[C28] Haisheng Zheng, Haoyuan Wu, **Zhuolun He**, Yuzhe Ma, and Bei Yu. iRw: An Intelligent Rewriting. *IEEE/ACM Proceedings Design, Automation and Test in Europe* (*DATE*), Lyon, France, Mar. 31–Apr. 2, 2025.

[C27] Yuan Pu, Fangzhou Liu, **Zhuolun He**, Keren Zhu, Rongliang Fu, Ziyi Wang, Tsung-Yi Ho, and Bei Yu. HeLO: A Heterogeneous Logic Optimization Framework by Hierarchical Clustering and Graph Learning. *ACM International Symposium on Physical Design* (*ISPD*), Austin, TX, USA, Mar. 16–19, 2025. *Best Paper Award Nomination*.

[C26] Haoyuan Wu, Haisheng Zheng, **Zhuolun He**, and Bei Yu. Parameter-Efficient Sparsity Crafting from Dense to Mixture-of-Experts for Instruction Tuning on General Tasks. *Empirical Methods in Natural Language Processing* (*EMNLP*), Miami, FL, USA, Dec. 12–16, 2024.

[C25] Yuan Pu, **Zhuolun He**, Tairu Qiu, Haoyuan Wu, and Bei Yu. Customized Retrieval Augmented Generation and Benchmarking for EDA Tool Documentation QA. *IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD*), Newark, NJ, USA, Oct. 27–31, 2024. *Best Paper Award Nomination*.

[C24] Yuan Pu, Fangzhou Liu, Yu Zhang, **Zhuolun He**, Kai-Yuan Chao, Yibo Lin, and Bei Yu. Lesyn: Placement-aware Logic Resynthesis for Non-Integer Multiple-Cell-Height Designs. *ACM/IEEE Design Automation Conference* (*DAC*), San Francisco, CA, USA, June 23–27, 2024.

[C23] Jiaxi Jiang, Lancheng Zou, Wenqian Zhao, **Zhuolun He**, Tinghuan Chen, and Bei Yu. PDRC: Package Design Rule Checking via GPU-Accelerated Geometric Intersection Algorithms for Non-Manhattan Geometry. *ACM/IEEE Design Automation Conference* (*DAC*), San Francisco, CA, USA, June 23–27, 2024.

[C22] Fangzhou Liu, Zehua Pei, Ziyang Yu, Haisheng Zheng, **Zhuolun He**, Tinghuan Chen, and Bei Yu. CBTune: Contextual Bandit Tuning for Logic Synthesis. *IEEE/ACM Design, Automation and Test in Europe Conference* (*DATE*), Valencia, Spain, Mar. 25–27, 2024.

[C21] **Zhuolun He** and Bei Yu. Large Language Models for EDA: Future or Mirage? *ACM International Symposium on Physical Design* (*ISPD*), Taipei, Mar. 12–15, 2024.

[C20] Yuan Pu, Tinghuan Chen, **Zhuolun He**, Chen Bai, Haisheng Zheng, Yibo Lin, and Bei Yu. IncreMacro: Incremental Macro Placement Refinement. *ACM International Symposium on Physical Design* (*ISPD*), Taipei, Mar. 12–15, 2024. *Best Paper Award Nomination*.

[C19] Siting Liu, Jiaxi Jiang, **Zhuolun He**, Ziyi Wang, Yibo Lin, and Bei Yu. Routing-aware Legal Hybrid Bonding Terminal Assignment for 3D Face-to-Face Stacked ICs. *ACM International Symposium on Physical Design* (*ISPD*), Taipei, Mar. 12–15, 2024.

[C18] Haisheng Zheng, **Zhuolun He**, Fangzhou Liu, Zehua Pei, and Bei Yu. LSTP: A Logic Synthesis Timing Predictor. *IEEE/ACM Asian and South Pacific Design Automation Conference* (*ASPDAC*), Incheon, South Korea, Jan. 22–25, 2024.

[C17] **Zhuolun He** and Bei Yu. Heterogenous Acceleration for Design Rule Checking. *IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD*), San Francisco, CA, USA, Oct. 29–Nov. 2, 2023. *Invited Paper*.

[C16] Zehua Pei, Fangzhou Liu, **Zhuolun He**, Guojin Chen, Haisheng Zheng, Keren Zhu, and Bei Yu. AlphaSyn: Logic Synthesis Optimization with Efficient Monte Carlo Tree Search. *IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD*), San Francisco, CA, USA, Oct. 29–Nov. 2, 2023.

[C15] **Zhuolun He**, Haoyuan Wu, Xinyun Zhang, Xufeng Yao, Su Zheng, Haisheng Zheng, and Bei Yu. ChatEDA: A Large Language Model Powered Autonomous Agent for EDA. *ACM/IEEE Workshop on Machine Learning for CAD* (*MLCAD*), Snowbird, UT, USA, Sept. 11–13, 2023.

[C14] **Zhuolun He**, Yihang Zuo, Jiaxi Jiang, Haisheng Zheng, Yuzhe Ma, and Bei Yu. OpenDRC: An Efficient Open-Source Design Rule Checking Engine with Hierarchical GPU Acceleration. *ACM/IEEE Design Automation Conference* (*DAC*), San Francisco, CA, USA, July 9–13, 2023.

[C13] Zehua Pei, Wenqian Zhao, **Zhuolun He**, and Bei Yu. Bit-Level Quantization for Efficient Layout Hotspot Detection. *International Symposium of Electronics Design Automation* (*ISEDA*), Nanjing, China, May 9–11, 2023.

[C12] Wei Zhong, Zhenhua Feng, **Zhuolun He**, Weimin Wang, Yuzhe Ma, and Bei Yu. Enabling Efficient Design Rule Checking with GPU Acceleration. *IEEE/ACM Proceedings Design, Automation and Test in Europe* (*DATE*), Antwerp, Belgium, Apr. 17–19, 2023. *extended abstract*.

[C11] Yuxuan Zhao, Qi Sun, **Zhuolun He**, Yang Bai, and Bei Yu. AutoGraph: Optimizing DNN Computation Graph for Parallel GPU Kernel Execution. *AAAI Conference on Artificial Intelligence* (*AAAI*), Washington, DC, USA, Feb. 7–14, 2023.

[C10] **Zhuolun He**, Yuzhe Ma, and Bei Yu. X-Check: GPU-Accelerated Design Rule Checking via Parallel Sweepline Algorithms. *IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD*), San Diego, CA, USA, Oct. 30–Nov. 3, 2022.

[C9] Ziyi Wang, Chen Bai, **Zhuolun He**, Guangliang Zhang, Qiang Xu, Tsung-Yi Ho, Bei Yu, and Yu Huang. Functionality Matters in Netlist Representation Learning. *ACM/IEEE Design Automation Conference* (*DAC*), San Francisco, CA, USA, July 10–14, 2022.

[C8] **Zhuolun He**, Ziyi Wang, Chen Bai, Haoyu Yang, and Bei Yu. Graph Learning-Based Arithmetic Block Identification. *IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD*), Munich, Germany, Nov. 1–4, 2021.

[C7] **Zhuolun He**, Peiyu Liao, Siting Liu, Yuzhe Ma, and Bei Yu. Physical Synthesis for Advanced Neural Network Processors. *IEEE/ACM Asian and South Pacific Design Automation Conference* (*ASPDAC*), Tokyo, Japan, Jan. 18–21, 2021. *Invited Paper*.

[C6] **Zhuolun He**, Lu Zhang, Peiyu Liao, Yuzhe Ma, and Bei Yu. Reinforcement Learning Driven Physical Synthesis. *IEEE International Conference on Solid-State and Integrated Circuit Technology* (*ICSICT*), Kunming, China, Nov. 3–6, 2020. *Invited Paper*.

[C5] Rui Lin, Ching-Yun Ko, **Zhuolun He**, Cong Chen, Yuan Cheng, Hao Yu, Graziano Chesi, and Ngai Wong. Hotcake: Higher order tucker articulated kernels for deeper CNN compression. *IEEE International Conference on Solid-State and Integrated Circuit Technology* (*ICSICT*), Kunming, China, Nov. 3–6, 2020. *Invited Paper*.

[C4] **Zhuolun He**, Yuzhe Ma, Lu Zhang, Peiyu Liao, Ngai Wong, Bei Yu, and Martin D.F. Wong. Learn to Floorplan through Acquisition of Effective Local Search Heuristics. *IEEE International Conference on Computer Design* (*ICCD*), Hartford, CT, USA, Oct. 18–21, 2020.

[C3] Yuzhe Ma, **Zhuolun He**, Wei Li, Tinghuan Chen, Lu Zhang, and Bei Yu. Understanding Graphs in EDA: From Shallow to Deep Learning. *ACM International Symposium on Physical Design* (*ISPD*), Taipei, Mar. 25–Apr. 1, 2020. *Invited Paper*.

[C2] **Zhuolun He**, Hanxian Huang, Ming Jiang, Yuanchao Bai, and Guojie Luo. FPGA-based Real-time Super-resolution System for Ultra High Definition Videos. *IEEE International Symposium on Field-Programmable Custom Computing Machines* (*FCCM*), Boulder, CO, USA, Apr. 29–May 1, 2018.

[C1] **Zhuolun He** and Guojie Luo. FPGA Acceleration for Computational Glass-Free Displays. *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays* (*FPGA*), Monterey, CA, USA, Feb. 22–24, 2017.

Preprints

[P4] Fangzhou Liu, Peiyi Han, Jiawei Liu, Yuan Pu, **Zhuolun He**, Rongliang Fu, Tsung-Yi Ho, and Bei Yu. SynAct: A Reasoning-Acting Large Language Model Agent for Adaptive Synthesis Optimization. arXiv:2608.12751, 2026.

[P3] Haoyuan Wu, Xueyi Chen, Rui Ming, Jilong Gao, Shoubo Hu, **Zhuolun He**, and Bei Yu. ToTRL: Unlock LLM Tree-of-Thoughts Reasoning Potential through Puzzles Solving. arXiv:2505.12717, 2025.

[P2] Jiajun Qin, Yuan Pu, **Zhuolun He**, Seunggeun Kim, David Z. Pan, and Bei Yu. UniMoCo: Unified Modality Completion for Robust Multi-Modal Embeddings. arXiv:2505.11815, 2025.

[P1] Haoyuan Wu, Haisheng Zheng, Shoubo Hu, **Zhuolun He**, and Bei Yu. Architect of the Bits World: Masked Autoregressive Modeling for Circuit Generation Guided by Truth Table. arXiv:2502.12751, 2025.

Academic Service

Associate Editor, *Integration, the VLSI Journal* Dec. 2025 – Present

Earlier Research Experience

Shanghai AI Laboratory Shanghai, China
Research Intern *Sept. 2022 – Oct. 2023*

SmartMore Hong Kong
Research Intern *Jun. 2020 – Apr. 2022*

The University of Hong Kong Hong Kong
Research Assistant *Nov. 2018 – Jul. 2019*

Technical Skills

Programming: C/C++, Python; CUDA, HLS-C, JavaScript/TypeScript, MATLAB, Rust.
Tools and frameworks: Bash, Bootstrap, LaTeX, PyTorch, Taskflow.